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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,584	04/22/2004	William Taylor	60027.0346US01/BS030286	6748

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EXAMINER	
SHIVERS, ASHLEY L	

ART UNIT	PAPER NUMBER
2609	

MAIL DATE	DELIVERY MODE
09/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/829,584	TAYLOR ET AL.	
	Examiner	Art Unit	
	Ashley L. Shivers	2609	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-28 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-28 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 22 April 2004 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

-- pages 1 and 17 attorney docket number "60027.0340US01/030259" should be "60027.0340US01/030276".

-- page 2 lines 14 the verb "be" should be removed after "may".

-- page 3 lines 2-3 repeats "while troubleshooting a network circuit" stated at the beginning of the same sentence.

-- page 13 line 15 "with" should be changed to "which".

-- page 18 line 10 "the renaming" is repeated.

-- page 18 lines 20 and 23 "Fig. 6" should be "Fig. 6A".

-- page 19 lines 9 and 12 make reference to a "Fig. 7" but that should be "Fig. 6B".

Appropriate correction is required.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the DLCIs, VPI/VCI, PVCs, and SVCs must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3-5, 7, 18, 20-22 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Hsing et al. **(U.S. Patent No. 6,167,025)**, hereinafter referred to as Hsing.

Regarding claim 1, Hsing discloses a method for automatically tracking the rerouting of logical circuit data in a data network **(Fig. 2, 200)**, the method comprising:

generating current reroute statistics upon the rerouting of logical circuit data from one or more failed logical circuits to one or more logical failover circuits in the data network **(See Fig. 5, 516 and Fig. 7A, 710)**, the current reroute statistics including trap data received for the one or more failed logical circuits in the data network **(See Fig. 2, 212)**.

generating a table for presenting the current reroute statistics without manual intervention **(See Fig. 2, 208, Figs. 3A-C)**;

generating updated rerouted statistics, the updated reroute statistics including updated trap data received for the one or more failed logical circuits in the data network **(See Fig. 7A, 720)**; and

updating the table with the updated reroute statistics without manual intervention **(See Fig. 2, 210 which updates the network information in the database)**.

Regarding claim 18, Hsing discloses a system for automatically tracking the rerouting of logical circuit data in a data network, the system comprising:

at least one network device for rerouting logical circuit data between one or more failed logical circuits to one or more logical failover circuits in the data network (**See Fig. 2, 204 and col. 8 lines 23-26**);

a logical element module, in communication with the at least one network device, for receiving trap data generated by the at least one network device (**See Fig. 2, 212 and col. 8 lines 47-48**); and

a network management module, in communication with the logical element module (**See Fig. 2, 205 and col. 8 lines 31-33**), for:

generating current reroute statistics upon the rerouting of logical circuit data from the one or more failed logical circuits to the one or more logical failover circuits (**See Fig. 5, 516 and Fig. 7A, 710**), the current reroute statistics including the trap data received by the logical element module (**See Fig. 2, 212**);

generating a table for presenting the current reroute statistics without manual intervention (**See Fig. 2, 208, Figs. 3A-C**);

generating updated reroute statistics, the updated reroute statistics including the trap data received from the logical element module (**See Fig. 7A, 720**); and

updating the table with the updated reroute statistics without manual intervention (**See Fig. 2, 210 which updates the network information in the database**).

Regarding claims 3 and 20, Hsing further discloses the method/system of claims 1 and 18, wherein the updated reroute statistics are generated upon the restoration of the one or more failed logical circuits in the data network (**See Fig. 10, 1006 and 1014**).

Regarding claim 4, Hsing further discloses the method of claim 1, wherein each of the one or more failed logical circuits and each of the one or more logical failover circuits in the data network is identified by a logical circuit identifier (**See Fig. 18B, 1802 and col. 15 lines 6-10**).

Regarding claim 5, Hsing further discloses the method of claim 4, wherein the trap data comprises the logical identifier for each of the one or more failed logical circuits and the logical identifier for each of the one or more logical failover circuits (**See Fig. 18B, 1802 and col. 15 lines 6-10**).

Regarding claim 7, Hsing further discloses the method of claim 4, wherein the trap data comprises the number of hops taken by each of the one or more logical failover circuits (**See Fig. 18B, 1802 and col. 15 lines 6-14**).

Regarding claim 21, Hsing further discloses the system of claim 18, wherein each of the one or more failed logical circuits and each of the one or more logical failover circuits in the data network is identified by a logical circuit identifier (**See Fig. 18B, 1802 and col. 15 lines 6-10**).

Regarding claim 22, Hsing further discloses the system of claim 21, wherein the trap data comprises the logical identifier for each of the one or more failed logical circuits and the logical identifier for each of the one or more logical failover circuits (**See Fig. 18B, 1802 and col. 15 lines 6-10**).

Regarding claim 24, Hsing further discloses the system of claim 21, wherein the trap data comprises the number of hops taken by each of the one or more logical failover circuits (**See Fig. 115, 1514 and col. 15 lines 6-14**).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsing in view of Bruno et al. **(U.S. Patent No. 5,894,475)** .

Regarding claims 2 and 19, Hsing teaches the method/system of claims 1 and 18, respectively, but fails to teach of the billing report.

Bruno teaches of the method/system of claims 1 and 18 further comprising generating a billing report including the updated reroute statistics **(See Fig. 3, 115-117 and col. 5 lines 24-27)**.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method/system of Hsing to include a billing system taught by Bruno in order to allocate a fee based system for the use of the network.

7. Claims 6 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsing.

Regarding claims 6 and 23, Hsing teaches the method/system of claims 4 and 21, respectively, but does not explicitly teach of the trap data comprising a current utilization of each of the one or more logical failover circuits.

However it would have been obvious to one of ordinary skill in the art at the time of the invention, to utilize the additional information field shown in **See Fig. 18B, 1802 and col. 15 lines 20-21** because it is not limited to specific aspects of the invention.

8. Claims 10, 12-17 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsing in view of Ashton et al. (**U.S. Patent No. 6,181,679**), hereinafter referred to as Ashton.

Regarding claims 10 and 27, Hsing teaches the method/system of claims 4 and 21 but fails to teaches of the logical circuit identifier being a DLCI.

Ashton teaches the method/system of claims 4 and 21, wherein the logical circuit identifier is a data link connection identifier (DLCI) (**See col. 6 lines 52-55**).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method of Hsing to include the logical circuit identifier being a data link connection identifier taught by Ashton in order to tell the network how to route the data.

Regarding claims 12-17, Hsing teaches the method of claim 1, but fails to teach of the circuit being a PVC or SVC and of the type of data network being used.

Regarding claims 12, 13 and 14, 15, Ashton teaches the method of claim 1, wherein at least one of the one or more logical circuits and logical failover circuits is a permanent virtual circuit (**See col. 6 lines 3-7**) or a switched virtual circuit (**See col. 6 lines 3-7**), respectively.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method of Hsing in view of Ashton to include the logical circuit being a PVC and SVC taught by Ashton in order to save time establishing new circuits.

Regarding claims 16 and 17, Ashton teaches the method of claim 1, wherein the data network is a frame relay network (**See col. 4 lines 55-57**) or an asynchronous transfer mode (ATM) network (**See col. 4 lines 57-61**), respectively.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method of Hsing to include the data network being a frame relay or ATM network taught by Ashton in order to emphasize the various types of networks that can be implemented.

9. Claims 11 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsing in view of Chen et al. (**U.S. PGPub No. 2005/0013242**), hereinafter referred to as Chen.

Regarding claims 11 and 28, Hsing teaches the method/system of claims 4 and 21, respectively, but fails to teach of the circuit identifier being a VPI/VCI.

Chen teaches of the logical circuit identifier is a virtual path/virtual circuit identifier (VPI/VCI) (**See [0004] lines 27-32**).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method and system of Hsing to include the logical circuit identifiers being virtual path/ virtual circuit identifiers taught by Chen in order to provide the identification of the circuit and the path that the circuit will take in the ATM network.

10. Claims 8, 9, 25, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsing in view of Bryenton **(U.S. Patent No. 6,826,184)**, hereinafter referred to as Bryenton.

Hsing teaches the method/system of claims 4 and 21, respectively, but fails to teach of the quality of service parameters of claims 8, 9, 25 and 26.

Regarding claims 8 and 25, Bryenton teaches the method/system of claims 4 and 21, respectively, wherein the trap data comprises a quality of service parameter for each of the one or more logical failover circuits **(See col. 5 lines 2-4 and lines 10-12)**.

Regarding claims 9 and 26, Bryenton teaches the method/system of claims 8 and 25, respectively, wherein the quality of service parameter comprises at least one of an unspecified bit rate; a variable bit rate; and a committed bit rate **(See col. 4 lines 63-67 and col. 5 lines 1-4)**.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention, to modify the method and system of Hsing to include the quality of service parameters taught by Bryenton in order to maintain a standard level for data transmission during rerouting.

Conclusion

11. Any response to this action should be **faxed** to (571)273-8300 or **mailed** to:

Commissioner of Patents,
P.O. Box 1450
Alexandria, VA 223103-1450

Hand delivered responses should be brought to:
Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ashley L. Shivers whose telephone number is (571) 270-3523. The examiner can normally be reached on Monday-Thursday 8:30-7:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Benny Tieu can be reached on (571) 272-7490. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AS

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